NPS ARCHIVE
1999.03
LINK, J.

NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

DESIGN OF A SERIAL COMMUNICATION PROTOCOL AND BUS INTERFACE CHIP FOR TACTILE COMMUNICATIONS

by

Jeffrey P. Link

March 1999

Thesis Advisors: Douglas J. Fouts
Jon T. Butler

THESIS
L66346

Approved for public release; distribution is unlimited.

DUDLEY KNOX LIBRARY
NAVAL POSTGRADUATE SCHOOL
MONTEREY CA 93943-5101

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188.

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	March 1999	Master's Thesis

4. TITLE AND SUBTITLE
DESIGN OF A SERIAL COMMUNICATION PROTOCOL AND BUS INTERFACE CHIP FOR TACTILE COMMUNICATIONS

5. FUNDING NUMBERS

6. AUTHOR(S)
Jeffrey P. Link

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey, CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

Tactile communication requires rapid data transfer along a common bus. The developed communication protocol and application-specific interface chip enable precise control of multiple tactile transmitters (tactors) to convey information to military users. This extrapolation of the Tactile Situation Awareness System developed by the Naval Aerospace Medical Research Laboratory uses a serial data bus and individual interface chips to communicate commands with a minimum number of conductors. This thesis develops the communication protocol and the design of the Tactor Interface Chip (TIC). This work also includes a computer-driven tactile array controller and Parallel Port Data Modulator for TIC testing and demonstration.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Electronics, Tactile, Interface, Tactor, TSAS, Serial Communications	316
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18, 298-102

Approved for public release; distribution is unlimited.

DESIGN OF A SERIAL COMMUNICATION PROTOCOL AND BUS INTERFACE CHIP FOR TACTILE COMMUNICATIONS

Jeffrey P. Link
Lieutenant Commander, United States Navy
B.S., Iowa State University, 1985
M.A., Webster University, 1991

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1999

ABSTRACT

Tactile communication requires rapid data transfer along a common bus. The developed communication protocol and application-specific interface chip enable precise control of multiple tactile transmitters (tactors) to convey information to military users. This extrapolation of the Tactile Situation Awareness System developed by the Naval Aerospace Medical Research Laboratory uses a serial data bus and individual interface chips to communicate commands with a minimum number of conductors. This thesis develops the communication protocol and the design of the Tactor Interface Chip (TIC). This work also includes a computer-driven tactile array controller and Parallel Port Data Modulator for TIC testing and demonstration.

TABLE OF CONTENTS

I. INTRODUCTION 1

A. COMMUNICATING THROUGH TOUCH 2

B. TACTILE SITUATION AWARENESS SYSTEM BY NAMRL 3

C. DEVELOPING INTELLIGENT TACTORS 4

D. THESIS OUTLINE 5

II. COMMUNICATION PROTOCOL 7

A. DESIGN REQUIREMENTS 7

1. Required Output 7

2. System Configuration 8

B. CONTROL STRUCTURE 9

1. Address 9

2. Pulse Shape 9

C. COMMAND FORMAT 10

1. Address Command Word 10

2. Pulse Width Word 11

3. Repetition Period Word 12

D. BUS ARCHITECTURAL CONSIDERATIONS 12

1. Command Promulgation Speed 13

2. Parallel Bus 13

3. Serial Bus 14

E. ARCHITECTURAL DECISION AND JUSTIFICATION 15

F. TRANSMISSION PACKET FORMAT 15

G. PHYSICAL CONSTRUCTION REQUIREMENTS 16

1. TIC and Tactor Power 17

2. Command Data and Timing Signals 17

III. TACTOR INTERFACE CHIP SPECIFICATION AND DESIGN 19
A. DESIGN GOALS 19
B. OPERATIONAL CONCEPT 20
1. Serial Data Receiver 21
2. Command Decoder and Controller 21
3. Tactor Power Controller 21
C. OPERATIONAL DESCRIPTION 22
D. FUNCTIONAL MODULE DESIGN 23
1. Serial Data Receiver 23
2. Command Decoder and Controller 24
3. Tactor Power Controller 26
E. VERILOG® DESIGN VERIFICATION 27
1. Twelve-Bit Input Shift Register 28
2. Eight-Bit Data Latch 28
3. Input Stream Validity Check 29
4. Command Sequence Controller 31
5. Address Comparator 34
6. Address Reference 34
7. Pulse Width Register 35
8. Repetition Period Register 36
9. Power Control Logic 37
10. Power Oscillator 38
11. Pulse Width Down Counter 39
12. Repetition Period Down Counter 40
13. Clock Divider 41
F. STRUCTURAL COMPONENT DESIGN 42
1. Structural Circuit Optimization 43
2. Twelve-Bit Input Shift Register 44
3. Eight-Bit Data Latch 44

4. Input Stream Validity Check 44
5. Command Sequence Controller 45
6. Address Comparator 46
7. Address Reference 46
8. Pulse Width Register 46
9. Repetition Period Register 47
10. Power Control Logic 47
11. Power Oscillator 47
12. Pulse Width Down Counter 47
13. Repetition Period Down Counter 48
14. Clock Divider 49
G. ADVANCED DESIGN FEATURES 49
1. Multiple Command Packet Addressing 49
2. All-Call Address 50
3. Dual Reset Circuit 50
4. Selectable Oscillator Frequency 50
5. Selectable Address 50
H. ANIMATION OF TACTOR INTERFACE CHIP OPERATIONS 51
1. TIC Visual Representation 51
2. Animation Color Scheme 52
IV. TACTOR INTERFACE CHIP VLSI IMPLEMENTATION 55
A. COMPETING VLSI DESIGN CONSTRAINTS 55
1. Size 55
2. Power 55
3. Speed 56
B. CMOS FET TRANSISTOR SIZING 56
1. Determining PFET Size From NFET Size 56
2. Basic Response Timing 57
B. LOGIC ELEMENT DESIGN 59

C. COMBINED LOGIC COMPONENT CONSTRUCTION 59
E. MODULE ASSEMBLY 60
F. INPUT AND OUTPUT CONSIDERATIONS 60
G. COMPLETE TACTOR INTERFACE CHIP 61
H. COMPREHENSIVE SYSTEM TESTING 63

V. PARALLEL PORT DATA MODULATOR 65
A. CREATING A SERIAL COMMAND STREAM 65
B. PARALLEL PORT INTERFACING AND CONTROL 66
C. MODULATOR DESIGN SPECIFICS 68
D. CREATING A PRINTED CIRCUIT BOARD LAYOUT 69
E. PRINTED CIRCUIT BOARD MANUFACTURING 72
F. PRINTED CIRCUIT BOARD ASSEMBLY 73
G. SOFTWARE TO DRIVE THE COMMAND MODULATOR 74
H. COMMAND MODULATOR TESTING 75
I. MODIFICATIONS TO THE MODULATOR DESIGN 76

VI. TACTOR INTERFACE CHIP TESTING 77
A. VLSI CHIP RECEIPT FROM FABRICATION 77
B. VISUAL INSPECTION 78
C. OPERATIONAL CHECK USING COMMAND MODULATOR 78
D. COMPLETE SYSTEM RESIMULATION 79
E. SCANNING ELECTRON MICROSCOPE INSPECTION 79
F. CHARGED ELECTRON IMAGING 81
G. FURTHER TESTING 82

VII. REVISIONS TO THE COMMUNICATION PROTOCOL 83
A. EVALUATION OF REGISTER COMMAND PAIRS 83
B. TACTILE ARRAY SIZING 84
C. PROGRAMMABLE OSCILLATION FREQUENCY 84
D. COMMANDED RESET 85
E. REVISED COMMANDED STRUCTURE 85

VIII. INCORPORATION OF ADDITIONAL DESIGN FEATURES 87
A. IMPROVED BI-DIRECTIONAL CURRENT SWITCHING SCHEME 87
B. PROGRAMMABLE OSCILLATION FREQUENCY 89
C. WAVE SHAPE GENERATION USING DUTY CYCLE 90
D. REVISED COMMAND DECODER AND CONTROLLER 91

IX. CONCLUSIONS AND FURTHER WORK 93
A. TACTILE INTERFACE SYSTEM PERFORMANCE 93
1. Simulation Performance during Design Process 93
2. Parallel Port Data Modulator Performance 93
3. Manufactured TIC Performance 94
B. IMPROVEMENTS THAT ARE READY TO INCORPORATE 94
1. Expanded Communication Protocol 94
2. Shaped Oscillation Current 94
3. Programmable Frequency 95
C. RECOMMENDATIONS FOR NEXT VLSI LAYOUT 95
1. Elaborate Testing and Measurement Points 95
2. Timing with Up Counters and Comparators 95
D. PROSPECTS FOR FUTURE DEVELOPMENT 95
1. On-board Current Switching 95

2. Programmable Addressing 96
3. Two-Way Communications 96

APPENDIX A. TIC MODELING USING VERILOG 97
A. TACTOR INTERFACE CHIP 97
B. SERIAL DATA RECEIVER 100
1. Twelve-Bit Input Shift Register 102
2. Eight-Bit Data Latch 105
3. Input Stream Validity Check 107
C. COMMAND DECODER AND CONTROLLER 110
1. Command Sequence Controller 113
2. Address Comparator 117
3. Address Reference 120
4. Pulse Width Register 121
5. Repetition Period Register 124
D. TACTOR POWER CONTROLLER 127
1. Power Control Logic 129
2. Power Oscillator 131
3. Pulse Width Down Counter 133
4. Repetition Period Down Counter 136
5. Clock Divider 139
E. SUPPORT COMPONENTS 142
1. Clock with Parametric Half-Period 142
2. D flip-flop, positive edge triggered 143
3. Transmission Gate MUX 145

APPENDIX B. SYSTEM DESIGN SCHEMATICS 147
A. SERIAL DATA RECEIVER 147
1. Twelve-Bit Input Shift Register 147

2. Eight-Bit Data Latch 148
3. Input Stream Validity Check 148
C. COMMAND DECODER AND CONTROLLER 149
1. Command Sequence Controller 149
2. Address Comparator 150
3. Pulse Width Register 151
4. Repetition Period Register 152
D. TACTOR POWER CONTROLLER 153
1. Power Control Logic 153
2. Power Oscillator 153
3. Pulse Width Down Counter 154
4. Repetition Period Down Counter 155
5. Clock Divider 156

APPENDIX C. STRUCTURAL EVALUATION USING SPICE 157
A. GENERAL DEFINITION FILES 157
1. CMOS FET Model Parameters 158
2. Fundamental Logic Element Definitions 159
B. SERIAL DATA RECEIVER 164
1. Twelve-Bit Input Shift Register 167
2. Eight-Bit Data Latch 169
3. Input Stream Validity Check 172
C. COMMAND DECODER AND CONTROLLER 176
1. Command Sequence Controller 182
2. Address Comparator 185
3. Pulse Width Register 188
4. Repetition Period Register 191
D. TACTOR POWER CONTROLLER 194
1. Power Control Logic 198

2. Power Oscillator 198
3. Pulse Width Down Counter 200
4. Repetition Period Down Counter 203
5. Clock Divider 206

APPENDIX D. TACTILE INTERFACE ANIMATION PROGRAM 209
A. ANIMATION DESIGN 209
1. TIC Visual Representation 209
2. Animation Color Scheme 210
B. ANIMATION PROGRAMMING 211
1. Intelligent Tactor 212
2. Command Byte 216
3. TIC Demo 218
4. Demonstration Applet HTML File 221

APPENDIX E. VLSI LOGIC ELEMENT DESIGN 223
A. LOGIC ELEMENT SCHEMATICS 223
1. Inverter 223
2. Two Input NAND 223
3. Three Input NAND 224
4. Four Input NAND 224
5. Three Input AND 224
6. Four Input AND 225
7. Two Input NOR 225
8. Three Input NOR 225
9. Two Input XOR 226
10. Two Input XNOR 226
11. D Flip Flop with Clear 227
12. Two Input Multiplexer 227
B. LOGIC ELEMENT SPICE SIMULATIONS 227

1. Inverter 228
2. Two Input NAND 228
3. Three Input NAND 229
4. Four Input NAND 230
5. Three Input AND 231
6. Four Input AND 232
7. Two Input NOR 233
8. Three Input NOR 234
9. Two Input XOR 235
10. Two Input XNOR 236
11. D Flip Flop with Clear 237
12. Two Input Multiplexer 238

C. VLSI LAYOUT 239

1. Legend of Layout Layers 239
2. Inverter 240
3. Two Input NAND 241
4. Three Input NAND 242
5. Four Input NAND 243
6. Three Input AND 244
7. Four Input AND 245
8. Two Input NOR 246
9. Three Input NOR 247
10. Two Input XOR 248
11. Two Input XNOR 249
12. D Flip Flop with Clear 250
13. Two Input Multiplexer 251

APPENDIX F. PARALLEL DATA MODULATOR DESIGN 253

A. COMMAND MODULATOR DESIGN USING VERILOG® 253

1. Four-Bit Register with Equality and Parity Calculation 255

2. Control State Machine 256
3. Eight-to-One Multiplexer 259
B. COMMAND MODULATOR IMPLEMENTATION USING ABEL™ 261
1. Four-Bit Register with Equality and Parity Calculation 261
2. Control State Machine 263
3. Eight-to-One Multiplexer 265
C. COMMAND MODULATOR ELEMENT INFORMATION 267
1. Four-Bit Register with Equality and Parity Calculation 268
2. Control State Machine 271
3. Eight-to-One Multiplexer 274

APPENDIX G. COMMAND TRANSMISSION PROGRAM 277
A. PARALLEL PORT COMMAND TRANSMISSION 277

APPENDIX H. GOMAC CONFERENCE PAPER 279

LIST OF REFERENCES 285

INITIAL DISTRIBUTION LIST 287

LIST OF FIGURES

Figure 1. TSAS Tactor Control. 3
Figure 2. Local Tactor Control. 4
Figure 3. Composition of the Intelligent Tactor. 5
Figure 4. Tactor Current-Switching Structure. 8
Figure 5. Tactor Activation Parameters. 9
Figure 6. Standard USART data packet format. 16
Figure 7. TIC Functional Modules. 20
Figure 8. TIC Operating States and Transitions. 22
Figure 9. Serial Data Receiver Elements. 24
Figure 10. Partial clearing prevents Erroneous Command Detection. 24
Figure 11. Command Decoder and Controller Elements. 26
Figure 12. Tactor Power Controller Elements. 27
Figure 13. Alternate Structures for Realizing the Address Comparator. 43
Figure 14. Tactile Interface Animation Basics. 52
Figure 15. Tactile Interface Animation in Progress. 53
Figure 16. Inverter Response for Various PFET Widths. 57
Figure 17. Delay Circuit for Measuring Inverter Response. 58
Figure 18. Inverter Transmission Response for Delay Circuit. 58
Figure 19. Completed Tactor Interface Chip VLSI Design. 62
Figure 20. Layout Map of the Tactor Interface Chip VLSI Design. 63
Figure 21. Simulation Results from the Complete TIC Design. 64
Figure 22. Command Modulator Conceptual Design. 66
Figure 23. Parallel Port Connector with Pins Numbered. 68
Figure 24. Parallel Port Modulator Component Layout. 70
Figure 25. Parallel Port Modulator Top Layer Routing. 71
Figure 26. Parallel Port Modulator Bottom Layer Routing. 71
Figure 27. Command Modulator Top Layer after Machining. 73
Figure 28. Fully Assembled Command Modulator. 74
Figure 29. Command Modulator Output for 19 Command. 75

Figure 30. Command Modulator Output for 218 Command....76
Figure 31. Tactor Interface Chip Pin Assignments....78
Figure 32. Scanning Electron Microscope Images of Potential Shorts....80
Figure 33. Scanning Electron Microscope Images of Aluminum Oxidation....80
Figure 34. Scanning Electron Microscope Image of Mask Failure....81
Figure 35. Scanning Electron Microscope Images of Embedded Impurities....81
Figure 36. Tactor Current-Switching Structure....88
Figure 37. Initial Current Switching Pattern....88
Figure 38. Revised Current Switching Pattern....88
Figure 39. Generating the Oscillation Frequency with Revised Switching....89
Figure 40. Wave Shape Generation using a Duty Cycle Register....90
Figure 41. Revised Command Decoder and Controller module....91
Figure 42. TIC Test Bench Verilog® source code....97
Figure 43. TIC Behavioral model Verilog® source code....99
Figure 44. TIC Structural model Verilog® source code....99
Figure 45. Serial Data Receiver Test Bench Verilog® source code....100
Figure 46. Serial Data Receiver Behavioral model Verilog® source code....101
Figure 47. Serial Data Receiver Structural model Verilog® source code....101
Figure 48. Twelve-Bit Input Shift Register Test Bench Verilog® source code....102
Figure 49. Twelve-Bit Input Shift Register Behavioral model Verilog® source code....103
Figure 50. Twelve-Bit Input Shift Register Structural model Verilog® source code....104
Figure 51. Eight-Bit Data Latch Test Bench Verilog® source code....105
Figure 52. Eight-Bit Data Latch Behavioral model Verilog® source code....106
Figure 53. Eight-Bit Data Latch Structural model Verilog® source code....106
Figure 54. Input Stream Validity Check Test Bench Verilog® source code....107
Figure 55. Input Stream Validity Check Behavioral model Verilog® source code....108
Figure 56. Input Stream Validity Check Structural model Verilog® source code....109
Figure 57. Command Decoder and Controller Test Bench Verilog® source code....110
Figure 58. Command Decoder and Controller Behavioral model Verilog® source code...111
Figure 59. Command Decoder and Controller Structural model Verilog® source code....112

Figure 60. Command Sequence Controller Test Bench Verilog® source code. 113
Figure 61. Command Sequence Controller Behavioral model Verilog® source code. 114
Figure 62. Command Sequence Controller Structural model Verilog® source code. 116
Figure 63. Address Comparator Test Bench Verilog® source code. 117
Figure 64. Address Comparator Behavioral model Verilog® source code. 117
Figure 65. Address Comparator Structural model Verilog® source code. 118
Figure 66. Address Comparator Alternate Structural model Verilog® source code. 119
Figure 67. Address Reference Test Bench Verilog® source code. 120
Figure 68. Address Reference Behavioral model Verilog® source code. 120
Figure 69. Pulse Width Register Test Bench Verilog® source code. 121
Figure 70. Pulse Width Register Behavioral model Verilog® source code. 122
Figure 71. Pulse Width Register Structural model Verilog® source code. 123
Figure 72. Repetition Period Register Test Bench Verilog® source code. 124
Figure 73. Repetition Period Register Behavioral model Verilog® source code 125
Figure 74. Repetition Period Register Structural model Verilog® source code. 126
Figure 75. Tactor Power Controller Test Bench Verilog® source code 127
Figure 76. Tactor Power Controller Behavioral model Verilog® source code. 127
Figure 77. Tactor Power Controller Structural model Verilog® source code. 128
Figure 78. Power Control Logic Test Bench Verilog® source code. 129
Figure 79. Power Control Logic Behavioral model Verilog® source code. 130
Figure 80. Power Control Logic Structural model Verilog® source code. 130
Figure 81. Power Oscillator Test Bench Verilog® source code. 131
Figure 82. Power Oscillator Behavioral model Verilog® source code. 132
Figure 83. Power Oscillator Structural model Verilog® source code. 132
Figure 84. Pulse Width Down Counter Test Bench Verilog® source code. 133
Figure 85. Pulse Width Down Counter Behavioral model Verilog® source code. 134
Figure 86. Pulse Width Down Counter Structural model Verilog® source code. 135
Figure 87. Repetition Period Down Counter Test Bench Verilog® source code 136
Figure 88. Repetition Period Down Counter Behavioral model Verilog® source code 137

Figure 89. Repetition Period Down Counter Structural model Verilog® source code.....137
Figure 90. Clock Divider Test Bench Verilog® source code.....139
Figure 91. Clock Divider Behavioral model Verilog® source code.....140
Figure 92. Clock Divider Structural model Verilog® source code.....140
Figure 93. Clock with Parametric Half-Period Test Bench Verilog® source code. 142
Figure 94. Clock with Parametric Half-Period Behavioral model Verilog® source code...142
Figure 95. D flip-flop Test Bench Verilog® source code. 143
Figure 96. D flip-flop Behavioral model Verilog® source code.....144
Figure 97. Transmission Gate MUX Test Bench Verilog® source code. 145
Figure 98. Transmission Gate MUX Behavioral model Verilog® source code. 145
Figure 99. Structural Schematic for the Twelve-Bit Shift Register. 147
Figure 100. Structural Schematic for the Eight-Bit Data Latch. 148
Figure 101. Structural Schematic for the Input Stream Validity Check. 148
Figure 102. Structural Schematic for the Command Sequence Controller.....149
Figure 103. Structural Schematic for the Address Comparator. 150
Figure 104. Structural Schematic for the Pulse Width Register.....151
Figure 105. Structural Schematic for the Repetition Period Register. 152
Figure 106. Structural Schematic for the Power Control Logic.....153
Figure 107. Structural Schematic for the Power Oscillator.....153
Figure 108. Structural Schematic for the Pulse Width Down Counter.....154
Figure 109. Structural Schematic for the Repetition Period Down Counter. 155
Figure 110. Structural Schematic for the Clock Divider. 156
Figure 111. CMOS PFET and NFET SPICE model definitions.....158
Figure 112. Subcircuits for Fundamental Logic Element SPICE model definitions. 159
Figure 113. Serial Data Receiver SPICE model source code.....164
Figure 114. Serial Data Receiver SPICE model response.....166
Figure 115. Twelve-Bit Input Shift Register SPICE model source code.....167
Figure 116. Twelve-Bit Input Shift Register SPICE model response.....168
Figure 117. Eight-Bit Data Latch SPICE model source code. 169
Figure 118. Eight-Bit Data Latch SPICE model input. 170

Figure 119. Eight-Bit Data Latch SPICE model response. 171
Figure 120. Input Stream Validity Check SPICE model source code. 173
Figure 121. Input Stream Validity Check SPICE model input. 174
Figure 122. Input Stream Validity Check SPICE model response. 175
Figure 123. Command Decoder and Controller SPICE model source code 178
Figure 124. Command Decoder and Controller SPICE model Control response. 180
Figure 125. Command Decoder and Controller SPICE model Register response. 181
Figure 126. Command Sequence Controller SPICE model source code 183
Figure 127. Command Sequence Controller SPICE model response 184
Figure 128. Address Comparator SPICE model source code 186
Figure 129. Address Comparator SPICE model response 187
Figure 130. Pulse Width Register SPICE model source code 189
Figure 131. Pulse Width Register SPICE model response. 190
Figure 132. Repetition Period Register SPICE model source code. 192
Figure 133. Repetition Period Register SPICE model response. 193
Figure 134. Tactor Power Controller SPICE model source code 195
Figure 135. Tactor Power Controller SPICE model response 197
Figure 136. Power Oscillator SPICE model source code. 198
Figure 137. Power Oscillator SPICE model response. 199
Figure 138. Pulse Width Down Counter SPICE model source code. 201
Figure 139. Pulse Width Down Counter SPICE model response. 202
Figure 140. Repetition Period Down Counter SPICE model source code. 203
Figure 141. Repetition Period Down Counter SPICE model response 205
Figure 142. Clock Divider SPICE model source code. 207
Figure 143. Clock Divider SPICE model response 208
Figure 144. Tactile Interface Animation Elements. 210
Figure 145. Tactile Interface Animation in Progress. 211
Figure 146. Intelligent Tactor object JAVA source code. 212
Figure 147. TIC Command object JAVA source code. 216
Figure 148. Tactile Array Demonstration object JAVA source code. 218
Figure 149. Tactile Demonstration Applet HTML source code. 221

Figure 150. Inverter schematic.....223
Figure 151. Two Input NAND Gate schematic. 223
Figure 152. Three Input NAND Gate schematic. 224
Figure 153. Four Input NAND Gate schematic. 224
Figure 154. Three Input AND Gate schematic. 224
Figure 155. Four Input AND Gate schematic. 225
Figure 156. Two Input NOR Gate schematic.....225
Figure 157. Three Input NOR Gate schematic.....225
Figure 158. Two Input XOR Gate schematic.....226
Figure 159. Two Input XNOR Gate schematic.....226
Figure 160. D Flip Flop with Clear schematic. 227
Figure 161. Two Input Multiplexer schematic.....227
Figure 162. Inverter SPICE model source code.....228
Figure 163. Two Input NAND gate SPICE model source code.....228
Figure 164. Three Input NAND gate SPICE model source code.....229
Figure 165. Four Input NAND gate SPICE model source code. 230
Figure 166. Three Input AND gate SPICE model source code.....231
Figure 167. Four Input AND gate SPICE model source code. 232
Figure 168. Two Input NOR gate SPICE model source code.....233
Figure 169. Three Input NOR gate SPICE model source code.....234
Figure 170. Two Input XOR gate SPICE model source code.....235
Figure 171. Two Input XNOR gate SPICE model source code.....236
Figure 172. D Flip Flop with Clear logic element SPICE model source code. 237
Figure 173. Two Input MUX logic element SPICE model source code. 238
Figure 174. Inverter layout.....240
Figure 175. Two Input NAND Gate layout.....241
Figure 176. Three Input NAND Gate layout.....242
Figure 177. Four Input NAND Gate layout. 243
Figure 178. Three Input AND Gate layout.....244
Figure 179. Four Input AND Gate layout. 245
Figure 180. Two Input NOR Gate layout.....246

Figure 181. Three Input NOR Gate layout. 247
Figure 182. Two Input XOR Gate layout. 248
Figure 183. Two Input XNOR Gate layout. 249
Figure 184. D Flip Flop with Clear layout. 250
Figure 185. Two Input Multiplexer layout. 251
Figure 186. Test bench for Parallel Port Data Modulator Verilog® model source code. 254
Figure 187. Test bench for Four-Bit Register Verilog® model source code. 255
Figure 188. Four-Bit Register Verilog® model source code. 256
Figure 189. Test bench for Control State Machine Verilog® model source code. 257
Figure 190. Control State Machine Verilog® model source code. 258
Figure 191. Test bench for Eight-to-One Multiplexer Verilog® model source code. 259
Figure 192. Eight-to-One Multiplexer Verilog® model source code. 260
Figure 193. Four-Bit Register ABEL™ source code. 262
Figure 194. Control State Machine ABEL™ source code. 263
Figure 195. Eight-to-One Multiplexer ABEL™ source code. 266
Figure 196. Four-Bit Register Summary Information. 268
Figure 197. Control State Machine Summary Information. 271
Figure 198. Eight-to-One Multiplexer Summary Information. 274
Figure 199. Command Transmission Driver C++ source code 278
Figure 200. GOMAC Conference Paper (page 1 of 4). 280
Figure 201. GOMAC Conference Paper (page 2 of 4). 281
Figure 202. GOMAC Conference Paper (page 3 of 4). 282
Figure 203. GOMAC Conference Paper (page 4 of 4). 283